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DESIGN AND FABRICATION OF PHASE - LOCKED LOOP FREQUENCY SYNTHESIZER CIRCUIT

Tan Qiuhong *, Zhang Yongwei, Jiang Shaoquan

Yunnan normal university, kunming, yunnan province
**Corresponding author email: tanqiuhong1@126.com*

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ABSTRACT

This paper introduces the design and fabrication of phase-locked loop frequency synthesizer circuit based on ADF4351 chip. System master chip selection STM32F103C8T6, power chip selection AMS1117-3.3V, display part of the use of OLED12864 LCD screen, download the chip selection CH340G. The STM32F103C8T6 converts the set frequency value into the value of the register, and then configures the corresponding register in the ADF4351 through the three-wire serial communication. ADF4351 according to the value of the register, control the internal voltage-controlled oscillator to produce the required frequency, and then divided by the output divider, you can set the frequency. While the screen shows the output frequency size. The test output frequency is stable, the amplitude is larger.

1. INTRODUCTION

With the advent of the information age, the field of computers and high-speed communications is becoming increasingly high for frequency sources [1]. In the field of signal generation, the current large number of frequency synthesis technology [2]. Phase-locked loop frequency synthesis technology refers to a fixed high-precision, high-stability fixed frequency signal, and ultimately get the required frequency of a high-precision, high stability of the signal [3]. The method is a technical method for obtaining the required frequency by controlling the output frequency of the voltage controlled oscillator by a certain multiplication and division operation. With the development of semiconductor technology, phase-locked loop frequency synthesizer chip has also been greatly developed, the stability of the output frequency is getting higher and higher, the signal peak is also growing. The phase-locked loop frequency synthesizer circuit described below is based on the ADF4351 chip, which incorporates a voltage-controlled oscillator, using the latest charge pump technology.

2. PHASE-LOCKED LOOP FREQUENCY SYNTHESIZER PRINCIPLE

This paper designs a phase-locked loop frequency synthesizer based on the ADF4351 chip [4]. The block diagram of the design shown in Figure 1, first by the active crystal with a high stability, high precision frequency source, after the R divider frequency and then sent to the injector input. When the VCO is uncontrolled, the frequency generated by the free oscillation is sent to the injector input terminal after being divided by the N divider. The injector generates a control signal through the charge pump according to the two input signals [5]. The output signal of the reamer is filtered by a filter and becomes a DC signal with a small fluctuation. DC signal control voltage-controlled oscillator, so that change the output frequency, through the entire loop of the continuous adjustment of the VCO output gradually close to the required, and then after the output divider frequency is required after the frequency. The frequency of the active crystal output is fixed, R divider, N divider, output divider ratio by the ADF4351 chip internal register control. Microcontroller STM32F103C8T6 through the three-wire serial communication, you can configure the ADF4351 internal register, to set the output frequency size. The ADF4351 also has an output lock determination, and the Lock Detect output is low when the PLL frequency synthesizer outputs a lock.

3. SYSTEM DESIGN OF PHASE - LOCKED LOOP FREQUENCY SYNTHESIZER CIRCUIT

3.1. Hardware design

Hardware system block diagram shown in Figure 1

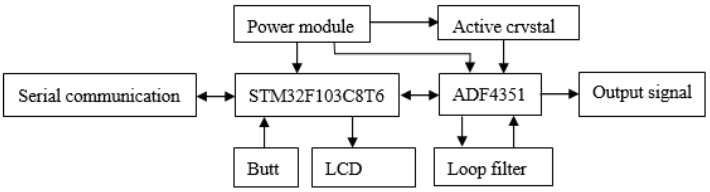

Figure 1: Hardware system block diagram

3.2. Microcontroller Module

In this paper, the design of the PLL frequency synthesizer, microcontroller selection STM32F103C8T6. The microcontroller is STM32F series in the low-end 32-bit ARM microcontroller. The chip. All I / O ports can be configured as external interrupts, providing great convenience for subsequent key program writing. And the kernel has single cycle multiplication and hardware division. The design according to their own needs, the design of the microcontroller module circuit shown in Figure 2.

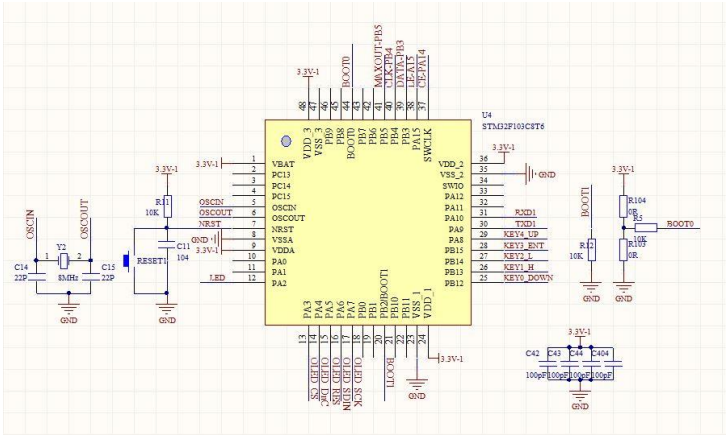

Figure 2: Microcontroller Circuit

3.3. Phase-locked loop chip and loop filter design

In this paper, the design of the PLL frequency synthesizer, choose to use ADF4351 chip [3]. The design in the hardware design is set to only one output leads to another differential output through the software set to mute. The chip 25 feet of the state for the Lock Detect, through the software configuration into Digital Lock Detect. In the pin connected to the LED lights, LED lights can be turned off to determine whether the output frequency is locked.

3.4. Serial communication module

The design of the serial communication chip used for CH340G. The design of the use of CH340G in the DTR and RTS BOOT0 were pulled up and reset, and through two transistors and other devices for level conversion, to achieve the program after the program automatically run. The circuit can be achieved either to download the program, you can also run the serial communication, the circuit shown in Figure 3.

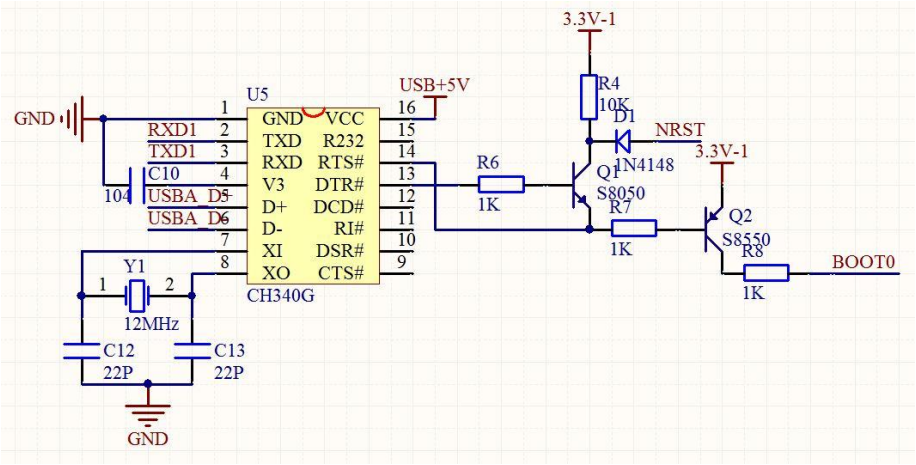

Figure 3: Serial communication circuit

3.5. Software program

The software program of this system should run on STM32F103C8T6 microcontrollers. Program to achieve through the five keys to set the phase-locked loop frequency synthesizer output frequency value, and throughout the operation of the OLED LCD screen to dynamic display, to achieve visual operation. As shown in Figure 8, the program in turn on the microprocessor, OLED screen and phase-locked loop chip initialization. After initialization, the frequency synthesizer output frequency of 100000kHz, and in the LCD screen display. The system waits for the key to be pressed to set the output frequency.

3.6. ADF4351 chip internal register parameter setting

According to the internal structure and the system's own design, the system uses 24MHz active crystal, the R register is configured as a fixed value of 240, that is, an input of the detector for a fixed 100KHz. The output frequency is changed by configuring the divider of the N divider and the output divider. The output divider size program is selected according to the size of the frequency set, ranging from 1 to 64. Set LD Pin Mode to Digital Lock Detect mode. You can determine whether the output frequency is locked by the LED light of the LD pin. Set the auxiliary output port of the ADF4351 chip to silent mode to set the output power to maximum. According to the above configuration, you can calculate the output of 100MHz when the ADF4351 chip 6 32-bit register values are 0X3E800000,0X800CB01,0X183C0E420, 0X4B3, 0XD0103C, 0X580005, the six values are also in the initialization of the microcontroller through the three-wire serial the value of the communication written to the ADF4351 chip.

4. TEST RESULTS

In order to verify the phase-locked loop frequency synthesizer circuit output signal was tested. Figure 10 is to set the output frequency of 100MHz output waveform, you can see the actual output frequency of 99.9937MHz, and set the value of less than 6KHz error. Figure 4 is a picture of a phase-locked loop frequency synthesizer with an output frequency of 111.1 MHz. Figure LCD screen shows the frequency of 111100KHz, loop lock indicator light, indicating the output lock. Figure 5 is to set the output frequency of 111.1MHz output waveform, we can see from the figure the actual output frequency of 111.097MHz, with the set value of 3KHz deviation. Figure 6 is to set the output frequency of 500MHz output waveform, we can see from the figure the actual output frequency and set the value of the deviation is very small. Figure 7 is to set the output frequency of 1GHz output waveform, the figure can be seen that the actual output frequency and set the value of the deviation is very small. Test shows that the output frequency of 35MHz to 200MHz, the output frequency deviation of less than 10kHz. The output frequency is less than 1MHz at 200MHz to 1GHz.

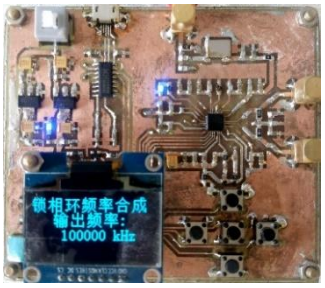

Figure 4: Output 100MHz display interface

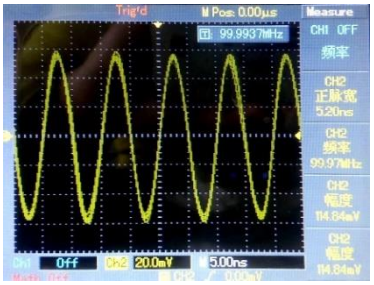

Figure 5: Output 100MHz output waveform

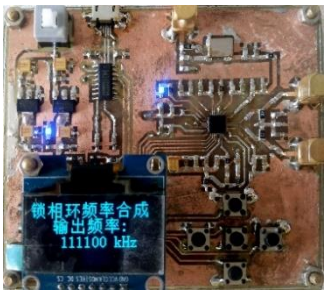

Figure 6: Output 111.1MHz display interface

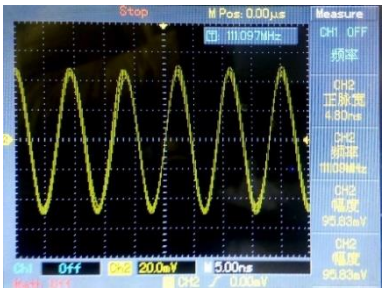

Figure 7: Output 111.1MHz output waveform

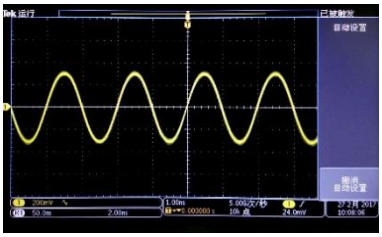

Figure 8: Output500MHz output waveform

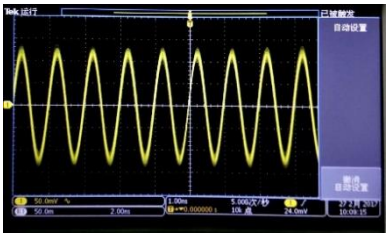

Figure 9: Output 1GHz output waveform

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5. CONCLUSIONS

This paper introduces the principle of phase-locked loop frequency synthesizer and the design process of hardware circuit and program of phase-locked loop frequency synthesizer based on ADF4351 chip. After testing the system to achieve the desired results, by the button to set the output frequency, in the process of setting the screen dynamic display settings process, to achieve visual operation. Output frequency range of 35MHz to 4.4GHz, and high precision and large amplitude.

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