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The principle of AD9920A and its application in CCD imaging system

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ABSTRACT

This design introduces the history and development of the CCD, and then introduces AD9920A chip was produced by Analog Devices, contain main features, working principle and its application in the imaging system. The AD9920A is a highly integrated CCD signal processor for digital still camera applications, which includes a complete analog front end (AFE) with analog-to-digital conversion, combined with a full-function programmable timing generator and 19 channel vertical driver, six GPOs that can be used for shutter and system functions, for accurate output timing of the clock signal of the CCD and the A / D conversion of the signal of the CCD.

1. Introduction

CCD application technology has become an important branch of electronic and optoelectronic science. CCD image acquisition system has important theoretical and practical significance for miniaturization and economy of the system. In the modern society of electronic technology, the application of image acquisition and processing technology The field is becoming more and more broad. The high degree of integration of the CCD image sensor greatly reduces the complexity of the system. It can integrate various functions into a chip as needed, not only can reduce the manufacturing cost, but also can quickly and collect and process the image.

2. THE CIRCUIT STRUCTURE OF CCD IMAGING SYSTEM

Charge-coupled devices (CCDs) are arrays of consisting of a small number of neat elements (commonly referred to as pixels) arranged in a neat array, with a total of about several hundred thousand or more [1]. Its role is equivalent to the photoreceptor cells on the human retina, used to feel the intensity of light on them above and color, CCD camera system block diagram shown in Figure 1, CCD device has the following characteristics:

(1) with a small size, light weight, low voltage and low power consumption, high reliability, long life, free from magnetic field interference, shock resistance and impact resistance and a series of advantages;

(2) with automatic scanning function, can be pixel addressing; the image of the fast response, distortion, size reproducibility and imaging fidelity, suitable for positioning, size measurement and imaging sensing and so on;

(3) digital scanning capabilities, digital code can determine the location of the pixel, easy and computer combination;

(4) the geometric accuracy of the sensor spacing is high, you can get a high positioning accuracy and measurement accuracy;

(5) high spatial resolution, photoelectric sensitivity, dynamic range.

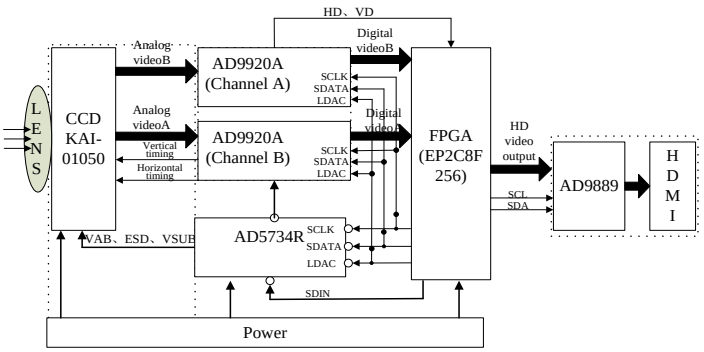

Figure 1: System block diagram of CCD camera

3. THE PRINCIPLE OF AD9920A AND ITS APPLICATION IN IMAGING SYSTEM

3.1. The principle of AD9920A

AD9920A driver generates the relevant timing signal, and then AD9920A output control timing to the CCD device to control the charge output of the CCD, CCD analog video signal after the incident to the AD9920A, after the AD9920A through CDS related dual sampling to eliminate noise interference, and then Through the gain amplifier VGA and then sent to the analog-to-digital converter ADC for analog conversion to 12bit digital video signal, and finally after the conversion of the digital signal to the next step to deal with [2]. Because the AD9920A integrates the timing generator and analog front end (AFE), it not only reduces the complexity of the circuit design and the size of the PCB, but also reduces the noise of the high-speed signal during transmission and processing and reduces the system power consumption.

3.2. The Configuration method of AD9920A

AD9920A chip register values are configured in two ways: one is the serial write operation, the other is a continuous serial write operation. The AD9920A is configured to complete the setting of the CDS sampling signal, the drive signal waveform, the gain of the variable gain amplifier, the clamp level and other function settings [3].

AD9920A implementation of the various functions in the internal register under the premise of the correct configuration, AD9920A chip internal register configuration is through a three-wire serial interface (SDATA, SCK, SL), AD9920A AFE register with the default value, the serial value of the serial write operation: when SL is low, the data is written, and the rising edge of each SCK clock is written as SDATA data, and the data is written continuously. 12-bit address signal and 28-bit data signal, SL rising edge SDATA data is latched, the serial write operation timing shown in Figure 2.

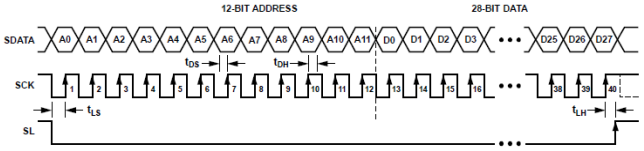

Figure 2: Serial Write Operation of AD9920A

3.3. Configuration of register values

The two AD9920A perform accurate output of the CCD clock signal and perform analog-to-digital conversion of the CCD signal. Since all drive clock and reset signals are provided by the AD9920A, the AD9920A's own registers are configured via the SPI interface to store a variety of clock drive patterns in advance. Two pieces of AD9920A chip in a pre-master mode, to provide the CCD needs of the clock and reset signal and electronic shutter signal, and channel A of the CCD signal acquisition; another piece of work in the post-Slave mode, the channel B Of the signal to collect, AD9920A circuit block diagram shown in Figure 3 [4].

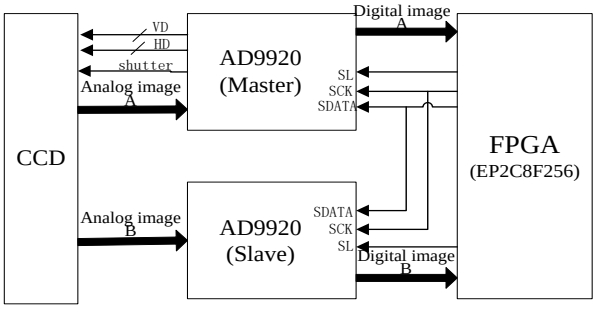

Figure 3: Block circuit diagram of AD9920A

4. THE EXTERNAL CIRCUIT DESIGN OF AD9920A

The AD9920A uses a flexible precision timer to generate high-speed timing signals, which are the basis for generating CCD and analog front-end timing, including reset gate (RG), horizontal drive, and SHP, SHD sampling clock. The edge of these signals can be programmed to control, accurate CCD horizontal output and analog front-end dual sampling to provide a guarantee for optimizing image quality, where AFE addresses 0x31 to 0x39 can set the horizontal signal mode, polarity, drive strength, RG, SHP, SHD polarity and length of time [5,6]. AD9920A chip image output interface shown in Figure 4, the horizontal signal driver circuit shown in Figure 1, three-wire configuration interface circuit shown in Figure 2, the vertical signal driver circuit shown in Figure 3.

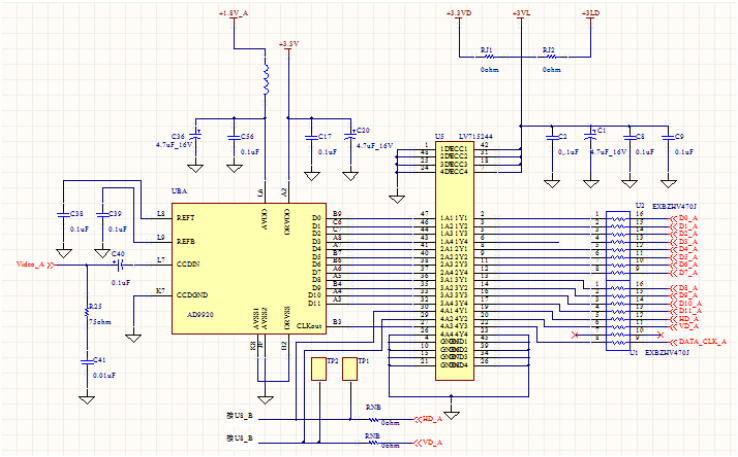

Figure 4: Image output interface of AD9920A

5. SYSTEM IMPLEMENTATION AND TESTING

Through the development of the hardware circuit debugging, troubleshooting hardware circuit, the preparation of the various procedures for experimental verification. The AD9920A in the configuration of the various registers, the test generated by the CCD drive signal timing are in line with KAI-01050 parameter requirements, Figure 5 shows the actual output of the video image.

Figure 5: The output image of testing

6. SUMMARY AND PROSPECT

In this paper, the performance, structure, working timing and power sequence of the AD9920A are described in detail. The analog front end of the AD9920A provides the level signal needed by the CCD chip and generates the vertical driving signal and the horizontal driving signal needed by the CCD device. And through the AD9920A chip internal A / D conversion module on the CCD output analog signal conversion, therefore, AD9920A will be applications in the domain of digital camera more and more widely.

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